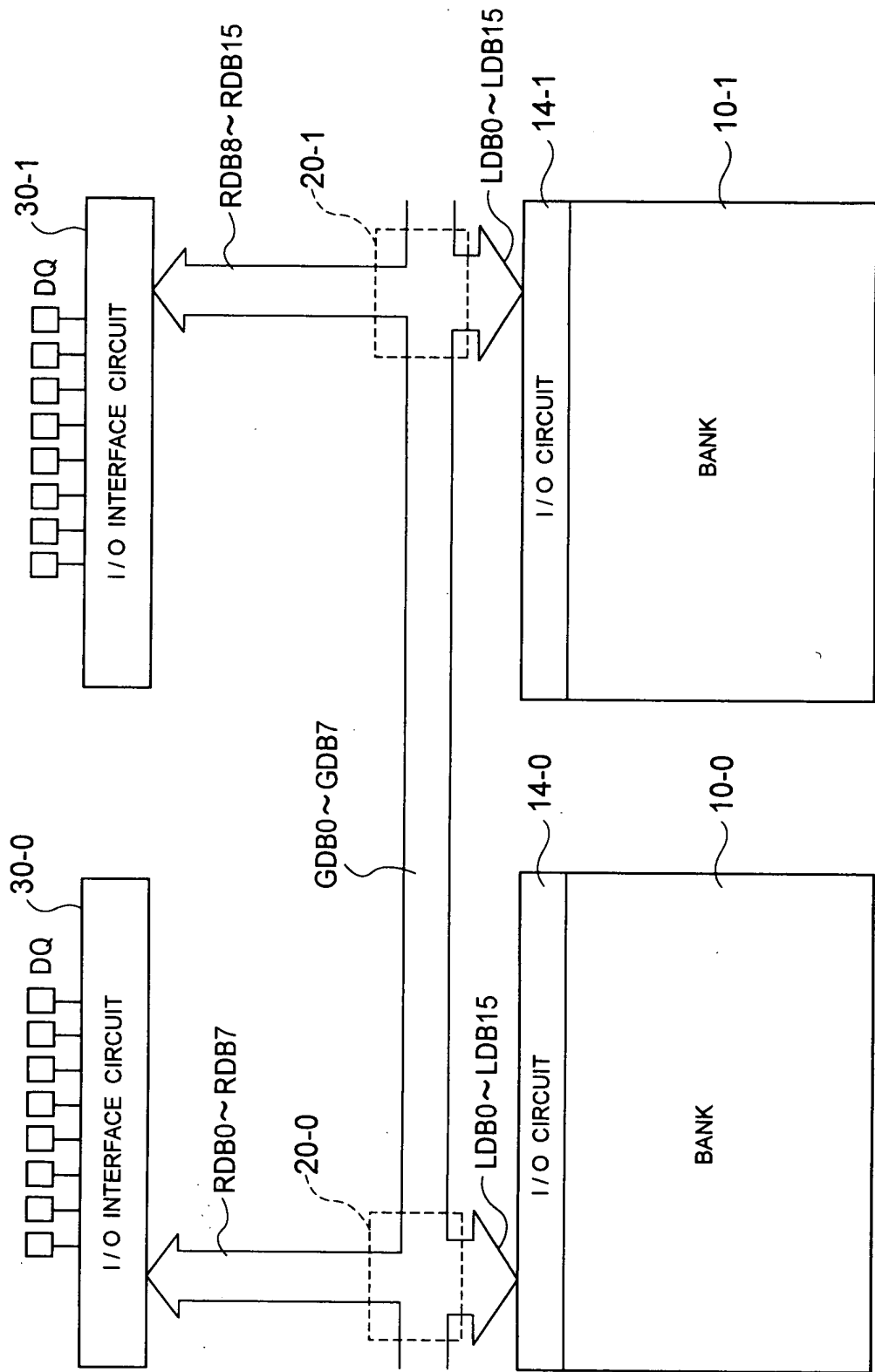




REPLACEMENT SHEET

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FIG. 1

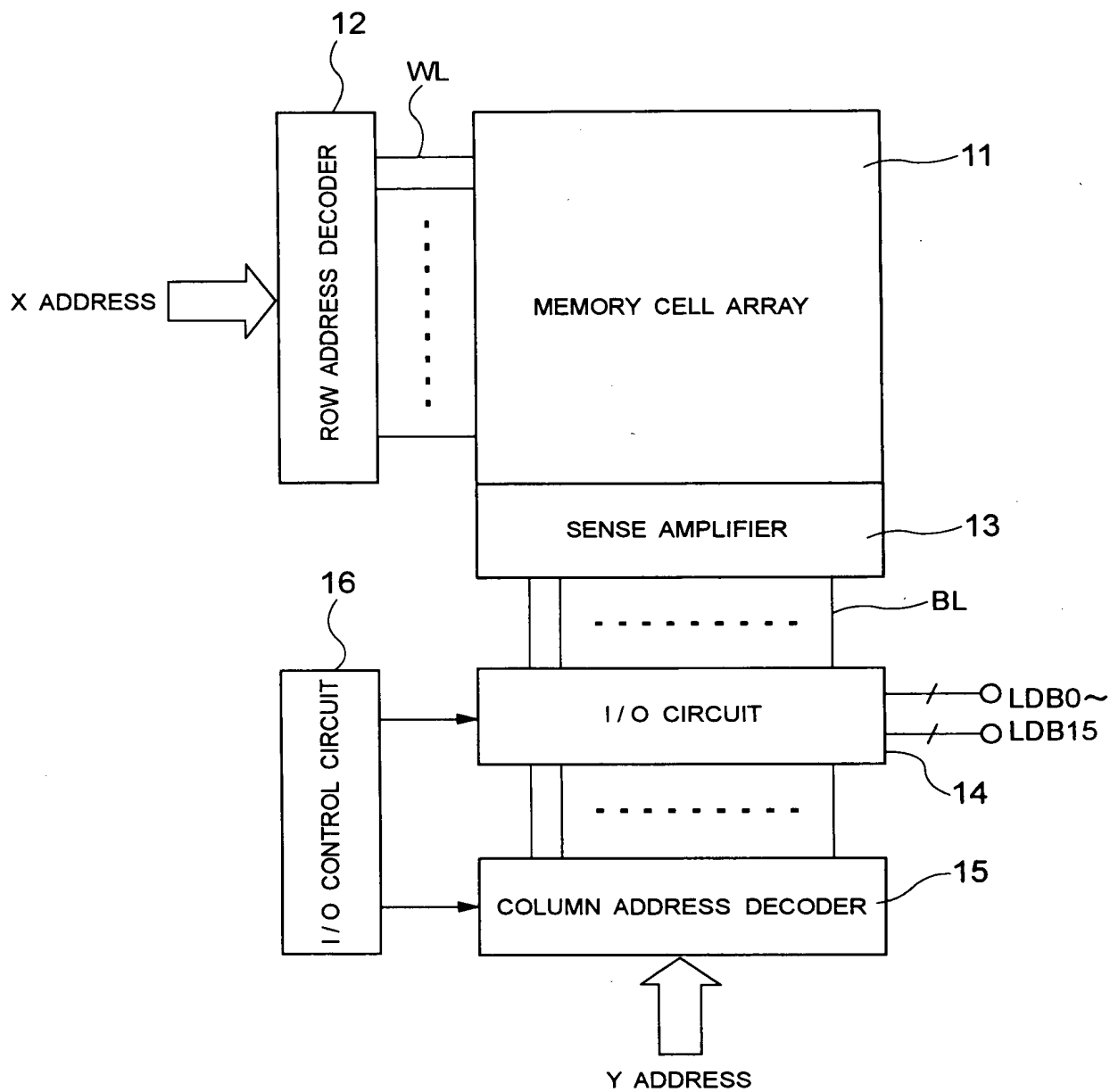




REPLACEMENT SHEET

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FIG. 2





REPLACEMENT SHEET

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FIG. 3

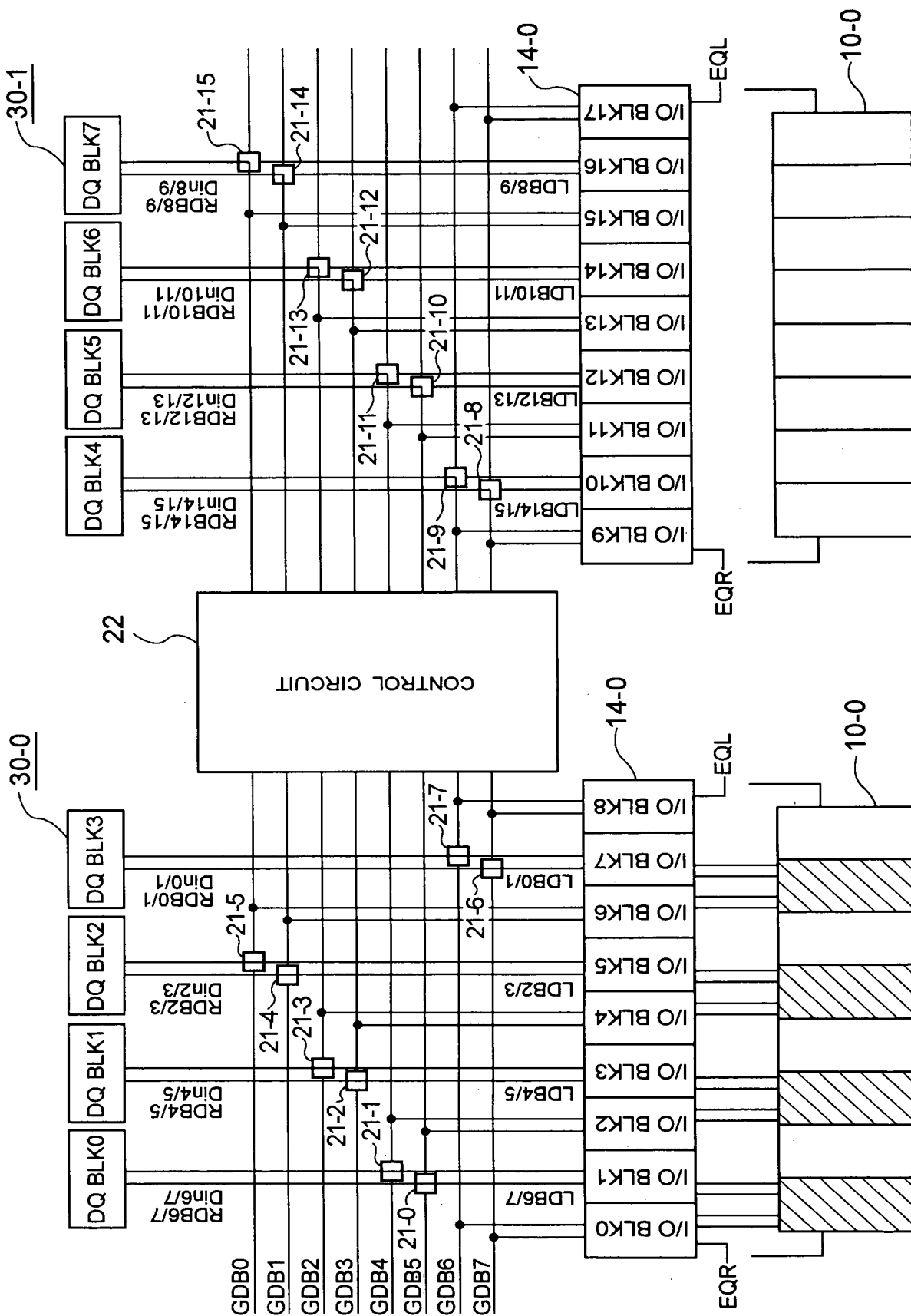


FIG. 4

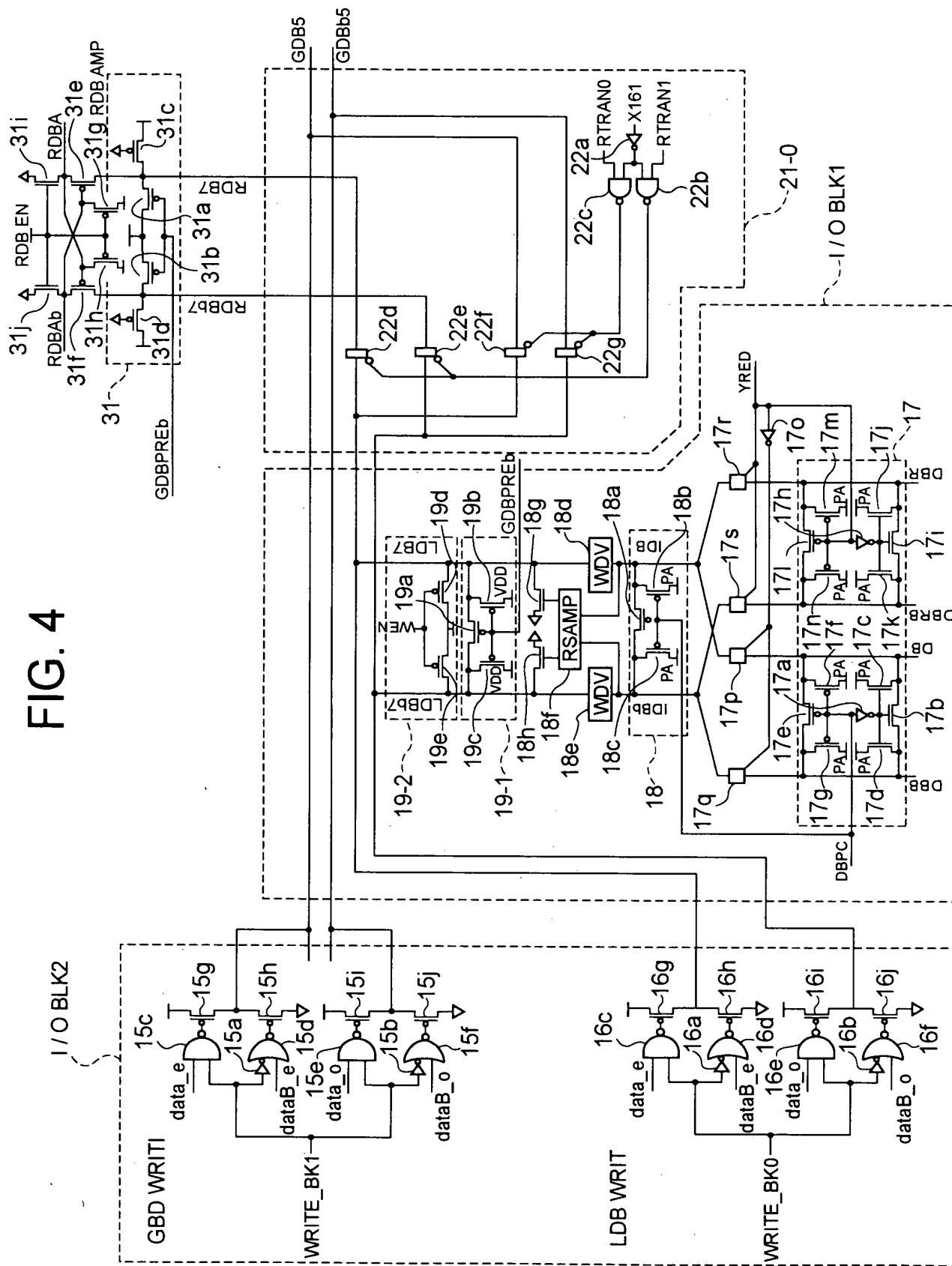


Figure 5 is a block diagram of a memory system. It features four banks of memory (10-1A, 10-1B, 10-2A, 10-2B) and four I/O interface circuits (30-0A, 30-0B, 30-1A, 30-1B). The banks are organized into two pairs, each with a BANK, I/O CIRCUIT, and I/O CIRCUIT. The I/O interface circuits are connected to the banks via data paths (solid lines) and control paths (dashed lines). The diagram also shows a central control unit (20-0A, 20-0B, 20-1A, 20-1B) and various control signals (GDB0~GDB3, RDB0~RDB3, LDB0~LDB7, RDB4~RDB7, LDB8~LDB15, DQ) that manage the data flow and control logic within the system.

